



The DLO4135/DLG4137 5 x 7 Dot Matrix Intelligent Display[®] Appnote 28

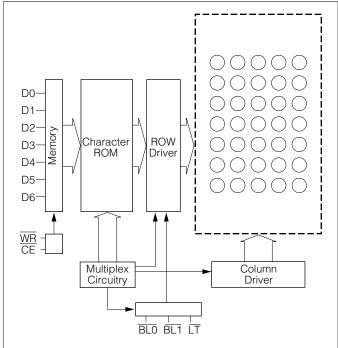
This application note is intended to serve as a design and application guide for users of the DLO4135 and DLG4137 OSRAM Intelligent Displays. This appnote covers device electrical description, operation, general circuit design considerations, and interfacing to microprocessors.

Electrical Description

The DLO4135/DLG4137 Intelligent Alphanumeric 5x7 Dot Matrix Display contains memory, character generator, multiplexing circuits, and drivers built into a single package.

Figure 1 is a block diagram of DLO4135/DLG4137. The unit consists of 35 LED die arranged in a 5x7 pattern and a single CMOS integrated circuit chip. The IC chip contains the column drivers, row drivers, 128 character generator ROM, memory, multiplex and blanking circuitry.

Figure 1. DLO4135/DLG4137 block diagram



Thirty-five dots form a 0.30 x 0.43 inch overall character size in a.500 x 1.00 inch dual-in-line package. The \pm 50 degree wide viewing angle complements the display and is the ideal display

© 2000 Infineon Technologies Corp. • Optoelectronics Division • San Jose, CA www.infineon.com/opto • 1-888-Infineon (1-888-463-4636) OSRAM Opto Semiconductors GmbH & Co. OHG • Regensburg, Germany www.osram-os.com • +49-941-202-7178 for industrial control applications. Display construction is filled reflector type with the integrated circuit in the back also filled with IC-grade epoxy. This results in a very rugged part which is resistant to moisture, shock and vibration.

Figure 2. Physical dimensions in inches (mm)

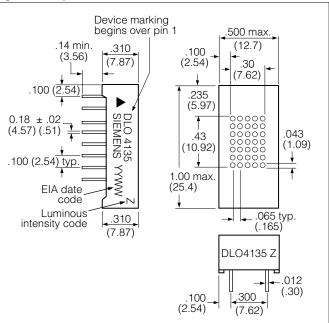


Table 1. DLO4135/DLG4137 pin functions

Pin	Function	Pin	Function
1	LT Lamp Test	9	D0 data LSB
2	WR Write	10	D1 data
3	BL1 Brightness	11	D2 data
4	BL0 Brightness	12	D3 data
5	No Pin	13	D4 data
6	No Pin	14	D5 data
7	CE Chip Enable	15	D6 data MSB
8	GND	16	+V _{CC}

Table 2. Pin description

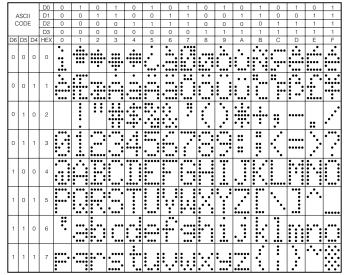
V _{CC}	Positive Supply +5 volts	
GND	Ground	
D0-D6	Data Lines, see Figure 3 (Character set)	
CE	Chip Enable (active low) This determines which device in an array will accept data	
WR	Write (active low) Data and chip enable must be present and stable before and after the write pulse (see data sheet for timing)	
BLO, BL1	Blanking Control Input (active low) Used to control the level of display brightness	
LT	Lamp Test (active low) Causes all dots to light at 1/2 brightness	

Operation

In a dot matrix display system, it is advantageous to use a multiplexed approach with 12 drivers (5 digit plus 7 segments) rather than 35 segment drivers. This obviously reduces the number of drivers and interconnections required. A multiplexed system must be a synchronous system, or the digits or elements may have different on (lit) times and therefore varying brightness.

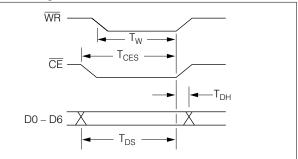
The DLO4135/DLG4137 is an internally multiplexed display, but the data entry is asynchronous. Loading data is similar to writing into a RAM. Present the data, select the chip, and give a write signal. For a multi digit system, each digit has its own unique address location and will display its contents until replaced by another code. The waveforms of Figure 4 shows the relationship of the signals required to generate a write cycle. Check the data sheet for minimum values required for each signal.

Figure 3. Character set



1. High=1 level. 2. Low=0 level

Figure 4. Timing characteristics



Display Blanking and Dimming

The DLO4135/DLG4137 Intelligent Display has the capability of three levels of brightness plus blank. Figure 5 shows the combination of $\overline{BL0}$ and $\overline{BL1}$ for the different levels of brightness. The $\overline{BL0}$ and $\overline{BL1}$ inputs are independent of write and chip enable and does not affect the contents of the internal memory. A flashing display can be achieved by pulsing the blanking pins at a 1–2 hertz rate. Either $\overline{BL0}$ or $\overline{BL1}$ should be held high to light up the display.

Table 3. Dimming and blanking control

Brightness Level	BL1	BL0	
Blank	0	0	
1/7 brightness	0	1	
1/2 brightness	1	0	
full brightness	1	1	

Lamp Test

The lamp test when activated causes all dots on the display to be illuminated at 1/7 brightness. It does not destroy any previously stored characters. The lamp test function is independent of chip enable, write, and the settings of the blanking inputs.

This convenient test gives a visual indication that all dots are functioning properly. The lamp test can be used as a cursor or pointer in a line of displays because it does not affect the display memory.

General Design Considerations

When using the DLO4135/DLG4137 on a separate display board having more than 6 inches of cable length, it may be necessary to buffer all of the input lines. A non-inverting 74LS244 buffer can be used. The object is to prevent current transient into the DLO4135/DLG4137 protection diodes. The buffers should be located on the display board and as close to the displays as possible.

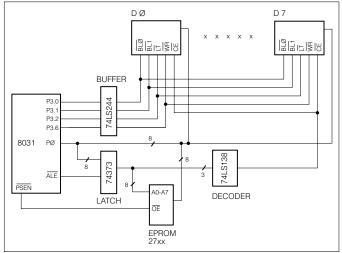
Because of high switching currents caused by the multiplexing, local power supply by-pass-capacitors are also needed in many cases. These should be 10 volt, tantalum type having 10 uf capacitance. The capacitors may only be required every 2 displays depending on the line regulation and other noise generators.

Decoupling capacitors should also be used across V_{CC} and ground of each display. Typical value of these capacitors is 0.01 mF/10 V.

If small wire cables are used, good engineering practice is to calculate the wire resistance of the ground and the +5 volt wires. More than 0.2 volt drop (at 100 ma per digit) should be avoided, since this loss is in addition to any inaccuracies or load regulation of the power supply.

The 5 volt power supply for the DLO4135/DLG4137 should be the same one supplying the V_{CC} to all logic devices. If a separate power supply must be used, then local buffers should be used on all the inputs. These buffers should be powered from the display power supply. This precaution is to avoid line transients or any logic signals to be higher than V_{CC} during power up.

Figure 5. Block diagram of the Intel 8031 controller



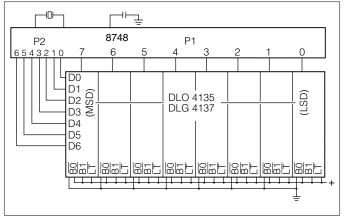
Interfacing

For an eight digit display using the DLO4135/DLG4137, interfacing to a single chip microprocessor such as the 8748, is easy and straight forward. One approach may be to dedicate one port for the seven data signals and another 8-bit port for the write signals. The schematic is shown in Figure 6.

I/O or Memory Mapped System

For a memory mapped system using a processor such as the 8080 or 8085, the interfacing is also straight-forward. Each display is treated as a memory location with its own address, like another I/O or RAM location. See Figure 7.

Figure 6. DLO4135/DLG4137 with 8748

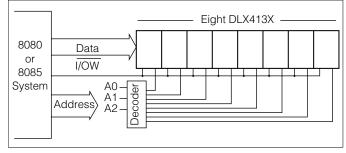


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Subroutine to Load an 8-digit Display using the DLO4135/ DLG4137

			; DATA IN RAM 10H-17H (MSD-LSD)
INIT	ORL ORL MOV MOV MOV	P1,#0FFH P2,#00H R1,#OFH R2,#0FEH R3,#08H	; PORT 1 ALL HIGH (WRITE) ; PORT 2 ALL LOW (DATA) ; RAM ADDRESS—1 ; WRITE PULSE : COUNTER
START: DATA:	INC MOV OUTL MOV RR MOV	R1 A,@R1 P2,A A,R2 A R2,A	; INCREMENT RAM POINTER ; FETCH DATA FROM RAM ; LOAD PORT 2 ; RECALL WRITE ; SHIFT A TO NEXT WRITE : SAVE WRITE
WRITE:	OUTL MOV OUTL DJNZ RET	P1,A A,#OFFH P1,A R3,START	; SEND WRITE PULSE ; WAIT ; RESET WRITE PULSE

Figure 7. Block diagram for 8-digit DLO4135/DLG4137



Routine for an 8-Digit Display using the DLO4135/DLG4137 and 8085 or 8080 Microprocessor

		-	; DATA TO BE DISPLAYED IS IN ; A0 (LSD) THRU A7 (MSD)
			; DISPLAY ADDRESS C00X ; LSD IS RIGHT MOST DIGIT
			, ; DOES NOT SAVE REG A,B,H,L,D,E
DADD DPAD	EQU EQU	0A000H 0C000H	, ; DATA ADDRESS LOCATION ; DISPLAY ADDRESS LOCATION
LEN	EQU	08H	; DISPLAY LENGTH
ORG	100H		
DISP:	LXI LXI MVI	H,DADD D,DPAD B,LEN	, ; LOAD DATA ADDRESS ; LOAD DISPLAY ADDRESS : LOAD DISPLAY LENGTH
DISP1:	MOV XCHG MOV XCHG INX INX DCR JNZ RET	A,M M,A D H B DISP1	; GET DATA ; XCHG H/L & D/E ; LOAD DISPLAY FROM REG A ; RESTORE H/L & D/E ; INCREMENT DISPLAY ADDRESS ; INCREMENT DATA ADDRESS ; DECREMENT LENGTH COUNTER ; END OF DISPLAY? ; RETURN TO MAIN PROGRAM

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Conclusion

Note that although other manufacturers' products are used in the examples, this application note does not imply specific endorsement, or warranty of other manufacturer's products by OSRAM. The interface schemes shown demonstrate the simplicity of using the DLO4135/DLG4137 dot matrix Intelligent Display. Slight timing differences may be encountered for various microprocessors, but can be resolved using similar methods as those used when using interfacing microprocessors with various RAMs. The techniques used in the examples were shown for their generality. The user will undoubtedly invent other schemes to optimize his particular system to its requirements.

Program Listing

II LISUING				
		; BY DAN WATSON		
		; TO DO LAMP TEST, SET 100% BRIGHTNESS		
		; AND WRITE STEIMENS*		
		· P3 0 = BL O\		
		; P3.2 = LT\		
		; P3.6 = WR\		
			LES - CE()	
		,		
		, II/ = II0 = II3 = WAIT REGISTERS		
0000		.ORG 00H		
0000	02 00 03	INIT: JMP BEGIN		
0003	12 00 24	BEGIN:CALL WAIT1	; DELAY FOR uC TO STABILIZE	
		MOV P3,#00H	; LAMP TEST	
			; DISPLAY LT\ FOR A WHILE	
			; SET ALL 8 DISPLAYS TO 100% BRT	
			; DIGIT 7 ADDRESS	
			; 8 DIGIT COUNTER	
0015	74 00	MOV A,#00H	; CLEAR ACC.	
0017	90 00 37	MOV DPTR,#TEXT	; ADDRESS OF THE MESSAGE	
001A	93			
			; DIGIT ADDRESS AND DATA WRITE	
			; NEXT CHARACTER ADDRESS	
			; NEXT DIGIT (6) ADDRESS	
			; WRITE ALL 8 CHAR.	
	00		, /	
0022	01 21	JMP GO	; MESSAGE ALWAYS ON	
0024				
			; DELAY LOOPS	
002A	7D FF			
002C	00	NOP		
002D	DD FE	DJNZ R5,\$		
	00			
0037	53 49 45 4D 45	TEXT:DB 'SIEMENS*'		
003C	4E 53 2A			
003F		.END		
	0000 0003 0006 0009 000C 000F 0010 0011 0013 0015 0017 001A 001B 0017 001A 001B 001C 001D 001E 001F 0021 0024 0024 0024 0024 0024 0024 0024	0000 02 00 03 0000 02 00 03 0003 12 00 24 0006 75 B0 00 0007 75 B0 07 0006 00 00 00 0010 00 00 00 0011 78 00 00 0013 79 08 00 0015 74 00 00 0017 90 00 37 001A 93 018 F2 001C A3 001D 08 001E E4 00 00 0021 00 00 00 0022 01 21 00 0024 7F 88 0026 0024 00 00 00 0024 7D FF 00 0025 00 00 00 0026 00 00 00 0027 7E FF 0	 BY DAN WATSON TO DO LAMP TEST, SET 100% BRIG AND WRITE 'SIEMENS*' P3.0 = BLO\ P3.1 = BL1\ P3.2 = LT\ P3.2 = LT\ P3.2 = UR R7 = R6 = R5 = WAIT R7 = R6 = R5 = WAIT R7 = R6 = R5 = WAIT R7 = R6 = R5 = WAIT REGISTERS 0000 02 00 03 INIT.JMP BEGIN 0003 12 00 24 BEGIN:CALL WAIT1 0006 75 80 00 MOV P3,#00H 0007 58 00 0 MOV P3,#00H 0008 75 80 07 MOV P3,#07H 0006 00 NOP 0010 00 NOP 0011 78 00 MOV R0,#00H 0013 79 08 MOV R1,#08H 0015 74 00 MOV A,#00H 0017 90 00 37 MOV DPTR,#TEXT 001A 93 WRT:MOVC A,@A+DPTR 001D 08 INC R0 001E E4 CLR A D01F D9 F9 DJNZ R1,WRT 0021 00 GO:NOP 0022 01 21 JMP GO 0024 0024 005 7E FF WAIT1:MOV R7,#88H 0026 00 NOP 0027 7E FF WAIT2:MOV R6,#FFH 0020 00 NOP 0021 00 GO:NOP 0022 01 21 JMP GO 0024 004 NOP 005 005 NOP 006 NOP 007 008 INC R0 009 009 000 000	